REMARKS

Applicants have cancelled claims 13-24 and amended claims 1 and 25 to clarify that the claim term "connected" means "electrically in contact" in many of the contexts in which "connected" was used. No new matter has been added, nor has any new issues been raised by this mere clarification of claim language.

Claim 25 has been rejected under 35 USC 102(b) as anticipated by U.S. Patent No. 6,124,736 (Yamashita). This rejection is respectfully traversed.

The semiconductor switching circuit device of claim 25 receives two pairs of signals at corresponding input terminal pads and outputs only one of the two pairs as the output signals from the corresponding common output terminal in response to the control signals received at corresponding control terminal pads, as explained at page 4 of the amendment filed March 17, 2003. Thus, the same signals as received at the input terminal pads are outputted from the output terminals as the output signals. Claim 25 as amended explicitly recites this feature as "the source electrode or the drain electrode of each of the two transistors of the first switch being electrically in contact with the common output terminal pad of the first switch." The claim also recites the same feature for the second switch of the claimed semiconductor switching circuit device. Because the source or drain electrode is electrically in contact with the common output terminal pad, the same signal as inputted into the switch is inherently outputted from the common output terminal pad. Though applicants believe that the expression "connected to" appeared in claim 25 originally presented essentially has the same technical scope as the expression "electrically in contact with" introduced to replace the former expression in this amendment, applicants have amended the claim simply so that this difference between the claimed device and the prior art device is clear to the Examiner.

To reject claim 25 in the outstanding Action, the Examiner repeats the same arguments as set forth in the previous Action, dated December 18, 2002. In response to applicants' argument in the amendment filed March 17, 2003 that Yamashita's lead for the output signal 0' in Fig. 3b, which the Examiner cites as corresponding to the common output terminal of claim 25, is not connected to the source or drain electrode of the transistor, the Examiner contends at page 5, lines 10-15 of the Action, that Yamashita's lead is indirectly connected to the source or the gate. Applicants submit that the issue is not whether the two elements of the claimed device are directly or indirectly connected, rather whether the two elements are electrically in contact with each other so that the output signal is the same as the input signal.

Clearly, Yamashita's device is a logic circuit device, as the title of Yamashita indicates. Accordingly, the transistors in Yamashita's logic circuit are silicon-based field effect transistors, i.e., MOSFETs. Persons of ordinary skill in the art would have understood that Yamashita's transistors have a gate oxide film between the channel region and the gate electrode. Thus, Yamashita's leads are not electrically in contact with the corresponding source or drain of the logic circuit device. The signals inputted through Yamashita's leads I0, I0', I1, I1', which the Examiner cites as corresponding to the input terminal pads of claim 25, are not outputted from the output leads O, O' of Yamashita, because the input signals are applied to the gate electrodes of the corresponding MOSFET, which are not electrically in contact with, or connected to, to use the prior claim language, the corresponding output leads because of the intervening gate oxide film. Rather, the input signals applied to the corresponding gates of the transistors are inverted by the inverter circuit including MOSFETs T206-T209 so that inverted signals are outputted from the output leads O, O' of Yamashita. Accordingly, Yamashita does not teach or suggest the

feature of claim 25 that the source or the drain of the transistor is electrically in contact with the common output terminal.

Furthermore, in response to applicants' argument that the logic circuit C200 shown in Fig. 3b of Yamashita relied upon by the Examiner does not have any terminal pad for external connection because the logic circuit is a part of larger circuitry, the Examiner just states "Fig. 3b of Yamashita et al. does show the output signal O' is the common output terminal pad of its circuitry 200." See, for example, page 10, lines 2-4 of the Action. Applicants do not understand this statement at all. First, how the output signal O' can be a terminal pad? The Examiner is correct in identifying characters O, O' as signals. These characters O, O' in Fig. 3b indicate that those signals come out from the portion of wiring lines, or the leads, marked by the characters, but do not represent any physical structure such as terminal pads. Accordingly, applicants assume that the Examiner meant that the characters O, O' represent corresponding parts of the wiring lines. If that is so, applicants submit that persons of ordinary skill in the art would have understood that the wiring lines marked as O and O' would extend to other portions of the larger circuitry. Accordingly, such an extension of the wiring line does not require the terminal pad of claim 25, which is used for connection to devices external to the claimed switching device as best depicted in Fig. 5 of the specification. Applicants request the Examiner to provide evidence that the wiring lines O, O' of Yamashita correspond to the common terminal pads of claim 25 in the event that he maintains the same argument in the next Action.

Accordingly, the rejection of claim 25 under 35 USC 102(b) should be withdrawn.

Claims 1-5, 7, 8, 10-12 and 26 have been rejected under 35 USC 103(a) over Yamashita in view of the prior art description in the specification. This rejection is respectfully traversed.

Claim 1 as amended recites that the common output terminal pads are electrically in contact with the source or drain electrode of the corresponding transistor. As explained above with respect to the switching device of claim 25, Yamashita does not teach or suggest such common output terminal pads. To overcome the deficiencies of Yamashita, the Examiner tries to rely on the prior art description in the specification.

In response to applicants' argument that the Examiner provides no evidence of motivation to combine Yamashita's logic circuit manipulating digital signals of only "0" and "1" and the switching circuit of the prior art description selecting one high frequency analog signal in response to a control signal, the Examiner states, "One cannot show nonobviousness by attacking references individually where rejections are based on combination of references." However, applicants do attack Yamashita and the prior art description in the specification individually to show that none of the references provides the motivation to combine them.

In addition to the argument in the amendment filed March 17, 2003, applicants describe further the difference between Yamashita's logic circuit and the switching device of the prior art description in the specification to aid Examiner's understanding of the claimed invention. Yamashita's device is a digital logic circuit device. The logic is constructed by arranging logic signals running between the drain and the source and logic signals applied to the gate of the corresponding MOSFET. All these signals are digital signals. Accordingly, such circuits require power sources like the one labeled VDD in Fig. 3b of Yamashita. Currents must be supplied from this power source VDD to the inverter circuit T206-T209 for generating the converted signals. On the other hand, the switching device of the prior art description in the specification does not need such a designated power source because currents are supplied through the Schottky contact at the gate of MESFET, which is normally biased, to the entire device. This is

possible because the gate electrode of MESFET does not require a gate oxide film. The two energizing methods are not compatible to each other. In addition, handling of the analog signals such as in the claimed switching device is a technology totally different from the technology of handling of the digital signals such as in Yamashita's logic circuit. Thus, the MESFET switching device for analog signals of the prior art description of the specification and Yamashita's MOSFET digital logic circuit rely on totally different device designs so that persons of ordinary skill in the art would not have been motivated to combine the teachings of Yamashita and the prior art description of the specification without any specific motivation to do so.

Applicants request the Examiner to provide specific evidence in the prior art of a motivation to combine Yamashita and the prior art description in the specification despite the difficulty explained above. Simply stating that such a structure is conventional in the art as the Examiner did at page 12, lines 2-7, of the Action is not enough. As emphasized by the court in *In re Lee*, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002), the Examiner must present specific evidence of motivation, not the generalized evidence relied on in the pending Action:

> When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. See, e.g., *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the *Graham* factors).

Without such evidence, the rejection under 35 USC 103(a) fails.

Claims 2-5, 7, 8 and 10-12 depend from claim 1, and claim 26 depend from claim 25 which is patentable. Thus, the rejection of claims 1-5, 7, 8, 10-12 and 26 under 35 USC 103(a) should be withdrawn.

Claims 27 and 28 have been rejected under 35 USC 103(a) over Yamashita. This rejection is respectfully traversed.

First, although the Examiner contends that Yamashita teaches the common output terminal pads of claim 27, Fig. 3b of Yamashita relied upon by the Examiner shows no such terminal pads, as explained above. Second, the Examiner admits that Yamashita does not teach the configuration of the two SPDT switches recited in claim 27. Then, the Examiner states that it would have been obvious to form the two SPDT switch configuration of claim 27 because this structure is conventional in the art for forming the two-switching-element switch without providing evidence to support his contention. As explained above, SPDT switches receive a signal and outputs the same signal, but Yamashita's logic circuit cannot output the same signal inputted to the circuit. Applicants request the Examiner to provide evidence that persons of ordinary skill in the art would have included two SPDT switches into Yamashita's logic circuit in the manner recited in claim 27. Without such evidence, the rejection of claim 27 fails.

Thus, the rejection of claims 27 and 28 under 35 USC 103(a) should be withdrawn.

In light of the above, a Notice of Allowance is solicited.

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition

for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. 492322002400.

Respectfully submitted,

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By: _____

Barry E. Bretschneider
Registration No. 28,055

Morrison & Foerster LLP
1650 Tysons Boulevard, Suite 300
McLean, VA 22102-3915
Telephone: (703) 760-7743
Facsimile: (703) 760-7777